IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Changes to any amended claims are indicated by strikethrough and underlining. This listing also reflects any cancellation and/or addition of claims.

Claim 1 (currently amended). A tracing control method, comprising:

initiating tracing of data during execution of a program that includes a plurality of instructions, said tracing initiation being based on a first trace control command embodied in one or more instructions of said program; and

halting said tracing based upon a second trace control command embodied in one or more instructions of said program;

wherein said first trace control command and said second trace control command are operative to trigger tracing on and off without using one or more breakpoints.

Claim 2 (original). The tracing control method of claim 1, wherein said first trace control command generates a trace enable indication and said second trace control command generates a trace disable indication.

Claim 3 (original). The tracing control method of claim 2, wherein a trace control indication is embodied in a field of a trace control register that is written to upon execution of a trace control command.

Claim 4 (original). The tracing control method of claim 2, wherein said first trace control command is inserted in an entry point to a section of code, and said second trace control command is inserted in an exit point to said section of code.

Claim 5 (original). The tracing control method of claim 1, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program.

Claim 6 (currently amended). A method for tracing a section of program code, comprising:

executing a program that includes a plurality of instructions, said plurality of instructions including one or more trace control commands,

initiating tracing of data upon entering a section of code in said program, said tracing initiation being based on a first trace control command in said program; and

halting said tracing upon leaving a section of code in said program, said halting being based upon a second trace control command in said program;

wherein said first trace control command and said second trace control command are operative to trigger tracing on and off without using one or more breakpoints.

Claim 7 (original). The method of claim 6, wherein said first trace control command generates a trace enable indication and said second trace control command generates a trace disable indication.

Claim 8 (original). The tracing control method of claim 7, wherein a trace control indication is embodied in a field of a trace control register that is written to upon execution of a trace control command.

Claim 9 (original). The tracing control method of claim 6, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program.

Claim 10 (currently amended). A tracing system, comprising:

an embedded processor, said embedded processor including,

a processor core for executing instructions; and

trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced;

wherein said tracing system is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints.

Claim 11 (original). The tracing system of claim 10, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic.

Claim 12 (original). The tracing system of claim 11, wherein said trace capture block sends trace data to an off-chip trace memory.

Claim 13 (original). The tracing system of claim 11, wherein said hardware input signals are received by said trace generation logic from said trace capture block.

Claim 14 (original). The tracing system of claim 10, wherein said embedded processor further includes a trace memory.

Claim 15 (original). The tracing system of claim 10, wherein said software-settable trace control register includes a trace select field that indicates whether said trace generation logic operates based on controls provided by said hardware input signals or by said software-settable trace control register.

Claim 16 (original). The tracing system of claim 10, wherein said software-settable trace control register is set by trace control commands that are embodied in one or more instructions of a program.

Claim 17 (original). The tracing system of claim 16, wherein said trace control commands are included within said program prior to execution of said program.

Claim 18 (currently amended). A computer program product comprising:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input

signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced; and

a computer-usable medium configured to store the computer-readable program codes;

wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints.

Claim 19 (currently amended). A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced;

wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints.

Claim 20 (currently amended). A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and

trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced;

wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints.

Claim 21 (original). The method of claim 20, wherein computer-readable program code is transmitted to said computer over the Internet.